REMARKS/ARGUMENTS

In the Office Action mailed March 4, 2010, claims 1, 2, 4 – 13, and 15 – 20 were rejected. In response, Applicants have amended claims 15 and 18 and canceled claims 1, 2, and 4 – 13. Applicants hereby request reconsideration of the application in view of the amended claims and the below-provided remarks.

Claim Rejections under 35 U.S.C. 102 and 103

Claims 1, 2, 4, 5, and 8 – 12 were rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener et al. (U.S. Pat. Pub. No. 2004/0088513, hereinafter Biessener) in view of Deng et al. (U.S. Pat. No. 6,795,327, hereinafter Deng). Additionally, claims 6, 7, and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener in view of Deng and further in view of Kim et al. (U.S. Pub. No. 2001/0015905, hereinafter Kim). Claims 15 – 18 were rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener et al. (U.S. Pat. Pub. No. 2004/0088513, hereinafter Biessener) in view of Falik et al. (U.S. Pat. No. 7,318,129, hereinafter Falik). Claims 19 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Biessener in view of Falik and Kim.

Claims 1, 2, and 4 – 13 have been canceled thereby rendering their rejection moot.

With respect to claims 15 – 20, Applicants respectfully submit that claims 15 – 20 are patentable over Biessener, Falik, and Kim for the reasons provided below.

Independent Claim 15

Claim 15 has been amended to particularly point out that the interface has an address output to an address path and a data output to a data path and to the address path and to particularly point out that the word-select unit is connected to the data path and the section-select unit is connected in the address path. Support for the amendments can be found in Applicants' specification at, for example, paragraphs [0071] – [0076] and Figures 1 – 3 (U.S. Pub. No. 2006/0174056 A1). As amended, claim 15 recites:

"A memory device comprising:

an interface for receiving access requests, the interface having an address output to an address path and a data output to a data path, wherein address information is carried on the address path and data for writing to memory or data read from memory is carried on the data path;

a memory cell array having a plurality of low-latency, rewritable, non-volatile memory cells forming at least one memory section;

a word-select unit connected in the data path and to the address path and between the interface and the memory cell array to provide column selection;

a section-select unit connected to the address path and between the interface and the memory cell array to provide row selection;

wherein both the word-select unit and the section-select unit select a respective column and row of the memory cell array in response to the address information;

a profile storage unit connected to said interface comprising a plurality of request profiles that each represent a profile of an access request, wherein each request profile includes:

a set of request information elements, wherein at least one of the request information elements indicates whether an access request is a read request or a write request; and

an access flag whose state indicates whether a corresponding access request is allowed to access the memory or not allowed to access the memory;

an access control unit connected to said profile storage unit and said memory and configured to allow or reject an access request;

wherein said profile storage unit selects an access flag that corresponds to a request profile in response to an access request that fits the request profile; and

wherein the access control unit allows or rejects an access request in response to the access flag that is selected by the profile storage unit." (emphasis added)

Applicants assert that Biessener in view of Falik does not teach every limitation of amended claim 15. For example, Applicants assert that the Biessener in view of Falik fails to teach the word-select unit and the section-select unit as recited in amended claim 1.

In support of the rejection of claim 1 and with respect to the word-select unit, the Office action simply states, "inherent column logic of memory array." (Office action, page 8) However, this assertion of inherency is insufficient to support the rejection of claim 15 at least because the assertion of inherency is not properly supported by rationale or evidence, as required by the MPEP.

The MPEP states that the Examiner must provide rationale or evidence in order to show inherency. MPEP 2112(IV). More specifically, in relying on a theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to

reasonably support the assertion that an allegedly inherent characteristic necessarily flows from the teachings of the cited reference. Id. Moreover, the MPEP states that the possible occurrence of a result or characteristic is not sufficient to establish inherency of the asserted result or characteristic. Id.

The conclusion of inherency asserted in the Office action is not supported by any rationale or evidence. In particular, the statement, "inherent column logic of memory array," does not provide any basis in fact and/or technical reasoning. Therefore, Applicants assert that a *prima facie* case of obviousness has not been established with respect to amended claim 15.

In support of the rejection of claim 15 and with respect to the section-select unit, the Office action states, "logic addressing a partition/ lines of memory, i.e. claim's row, for partition as disclosed in table 1, par. 58." (Office action, page 8) However, Applicants assert that Biessener does not teach a section-select unit connected to an address path as recited in amended claim 15. In particular, Biessener does not distinguish between an address path and a data path as recited in amended claim 15.

Further, Applicants assert that Biessener does not teach a profile storage unit having "a set of request information elements, wherein at least one of the request information elements indicates whether an access request is a read request or a write request." (emphasis added) In support of the rejection of this limitation, the Office action states, "par 68, a read or write request from user inherently has read or write information." (Office action, page 9) Without addressing the validity of the Examiner's statement, Applicants assert that the provided logic does not address the actual language of the claim. The language of the claim states that the profile storage unit has "a set of request information elements, wherein at least one of the request information elements indicates whether an access request is a read request or a write request." The Examiner's logic simply does not address whether or not a profile storage unit has such a set of information. Rather, the Examiner's logic is directed to a read or write request of a user. Because, the Examiner's logic does not address the actual language of the claim, Applicants' assert that a *prima facie* case of obviousness has not been established.

Additionally, claim 15 has been amended recite, "wherein both the word-select unit and the section-select unit select a respective column and row of the memory cell

array in response to the address information." Applicants assert that Biessener in view of Falik fails to disclose word-select and section-select units that select a respective column and row of a memory cell array as recited in amended claim 15

For at least the above-identified reasons, Applicants assert that amended claim 15 is patentable over Biessener in view of Falik.

Dependent Claims 16 – 20

Claims 16 – 20 depend from and incorporate all of the limitations of independent claim 15. Applicants respectfully assert that claims 16 – 20 are allowable at least based on an allowable claim 15. Additionally, each of claims 16 and 18 may be allowable for further reasons.

Claim 16 recites in part that "the profile storage unit comprises a set of access flags, one access flag for each row address, such that each access flag governs the access to one row of the memory cell array." (emphasis added) Falik teaches bits that control write access "to a specific shared memory block." (Falik, col. 13, lines 33 – 35) However, Applicants assert that Falik is silent as to access flags for each row address of a memory cell array as recited in claim 16.

Claim 18 has been amended to conform to the amendment to claim 15. In particular, "*a* data path" has been amended to "*the* data path." Claim 18 recites in part that "the access control unit operates in the data path to admit or reject a flow of data to or from the memory cell array depending on the state of the corresponding access flag it receives from the profile storage unit." (emphasis added) Falik teaches a JTAG I/F (110) and a parallel I/F (111) that are used to access a memory (140). Additionally, Falik teaches that an access control unit (104) provides access control functionality. However, Falik does not teach that the access control (104) operates in the data path as recited in claim 18. With reference to Fig. 2 of Falik, the JTAG I/F (110) and the parallel I/F (111) are connected directly to the memory (140). While the access control (104) may be logically located between the JTAG I/F (110) and the parallel I/F (111), Applicants assert that Falik does not teach that the access control is in the data path as recited in claim 18.

CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amended claims, the new claims, and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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